of ±10V.

The digital word sensed by the probes is latched into the input data register by the input clock pulses (see the block diagram, (Fig. 6). This occurs on every clock pulse, regardless of the state of the qualifiers, the ARM input, or the selected display mode. Clock pulses are supplied from an external source, usually the system under test, and are subject to the same threshold recognition criterion as the data.

The pattern recognition logic looks at the input data register continuously, and when there is a match between the input data and the front-panel TRIGGER WORD switch register, the "local" flip-flop is triggered, initiating the data acquisition sequence if the instrument is in the LOCAL mode. The "trigger bus" line also attempts to rise, but will not do so if it is held down by any other instrument on the trigger bus. Each instrument connected to the trigger bus drives the bus with an open-collector circuit so the bus cannot rise until trigger conditions are met simultaneously by all bus-connected instruments. If the instrument is in the BUS mode, data acquisition is not initiated until the trigger bus rises.

The use of two trigger-generating flip-flops makes it possible to have two instruments bus-connected so data acquisition in one is dependent on trigger conditions being met in both instruments simultaneously, while the other, operated in the LOCAL mode, acquires data any time its own trigger conditions are met.

Generation of a trigger also starts the delay generator. The pattern trigger output remains true until the delay generator produces the delayed trigger pulse. If zero delay were selected, the delayed trigger would occur simultaneously with the pattern trigger.

TRIGGER ARM, if selected, disables the local and trigger bus flip-flops until an arming input sets the arm flip-flop. Then when trigger conditions are met, a pattern trigger output is generated and the arm flip-flop is reset.

Qualifiers

The QUALIFIER inputs may be used in either of two ways. When qualifying trigger words, the qualifiers effectively become part of the trigger word, making it 18 bits wide. The two qualifier bits, however, are not stored or displayed.

When qualifying the display, the qualifiers control the entry of data: words can be clocked into memory only when qualifying conditions are met. Similarly, the delay generator counts only those clock pulses that coincide with the qualifiers.

The Data Acquisition Cycle

When the display circuits relinquish control of the instrument, they issue a data acquisition command. This resets the trigger and delay generators and, if the instrument is in the START DISPLAY mode, resets the data index counter and the "start" and "end" flip-flops (Fig 6). The next qualified clock pulse switches the memory address lines to the address counter.

Occurrence of the trigger word sets the start flip-flop. This enables the data index counter, which is then incremented by each write pulse. The trailing edge of the write pulse also increments the address counter.

Each digital word latched into the input data register is written into memory at the address indicated by the address counter. This continues until the 16-state data index reaches full count, which resets the end flip-flop, gating off the write-enable pulses and stopping the loading of data into memory. The end flip-flop also sets the "data ready" line true, indicating to the display section that data is complete and ready for display.

When the instrument is operated in the END DISPLAY mode, the start flip-flop is preset, allowing the data index counter to run. When the data index counter reaches terminal count, it enables the end flip-flop. Data is acquired until the next occurring trigger, which stops data acquisition immediately and switches memory control to the display section.

The count in the data index counter at any instant indicates how many good words are in memory. The address counter points to the next address in memory to be accessed. The difference between these two counts is the address of the first word of the current data sequence. During the display cycle, the difference is added to the count in the display section's vertical counter. The result is the address of the next word to be read out of memory for display.

Generating the Table Display

Whenever the data acquisition circuits set the data ready line true, the display circuits take control of the memory and read out and display the memory contents.

Read out is serial, with memory addressing controlled by two four-bit counters (Fig. 7). The "vertical" counter indicates the word to be read and the "horizontal" counter, working through a 1-of-16 multiplexer, selects the bit within that word to be displayed.

The horizontal counter is driven by an internally-generated 50-kHz clock. When it reaches state 15, it increments the vertical counter and then resets. In this fashion, every bit address in memory is polled.

The CRT beam is positioned by digital-to-analog converters driven by the counters. The vertical counter digits are weighted so a wider step occurs on every other vertical address, spacing the lines on the CRT in pairs for easier reading. A still wider step occurs on every fourth line.